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NEW APPROACHES TO THE DIRECT MEASUREMENT OF CAPACITANCE

M. S. RAVEN

Department of Electrical and Electronic Engineering, The University of Nottingham, University Park, Nottingham, England

D. RAVEN

Electronic Services and Products (ESP) Ltd., Long March Industrial Estate, Daventry, Northants, England

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The limitations of conventional a.c. capacitance measuring techniques, for such measurements as MIS interface capacitance and measurements of large value electrolytics, has lead to a demand for new methods of capacitance measuring. This article reviews two new approaches which are presently being employed – the quadrature P.S.D. technique and time encoded ballistic techniques.

1. INTRODUCTION

Conventional a.c. methods of measuring capacitance, which incorporate the ratio arm transformer and variations of the Wheatstone Bridge, may be used to measure capacitance below 1 μF to a precision sufficient to establish secondary standards. However the instrumentation that is required to establish standards is not necessarily the same as that required in the broader areas of industry. This has always applied to the measurement of current, voltage and resistance but simple and direct methods of measuring capacitance have been neglected.

Over the past 2–3 years, however, alternative techniques have been applied to the measurement of capacitance. These techniques have been designed specifically to allow direct linear display of capacitance and its associated parameters. During this period there has also been rapid developments in the instrumentation field that directly influence the design of capacitance meters. First is the development of small calculator styled instruments and second is the development of microprocessor controlled component measuring instruments.

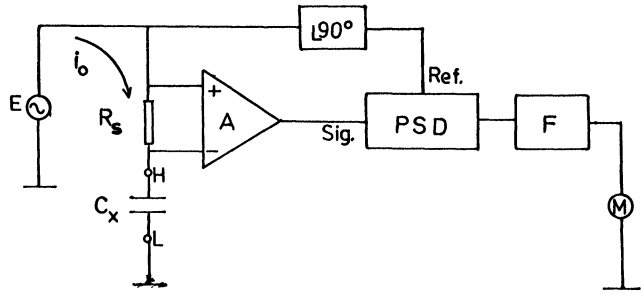

FIGURE 1 Schematic circuit diagram of a PSD Capacitance Meter. A – main instrumentation amplifier. 90° – phase shifting network. PSD – phase sensitive detector. F – filter. M – meter circuit.

In this paper we consider two measuring principles which are the most commonly employed in modern direct reading capacitance meters. These are the quadrature or phase sensitive detection methods[1] and the time encoded ballistic methods.[2]

2. PHASE SENSITIVE DETECTION METHODS

In this technique the capacitor to be tested, C_x, is connected in series with a fixed resistor, R_s, driven from a constant amplitude, constant frequency, sine wave source, Figure 1. The voltage drop across R_s is sensed by a differential amplifier and the output applied to a phase sensitive detector (PSD). For capacitative measurements the PSD reference signal is obtained from the oscillator output via a 90 degrees phase shifting network. The output signal from the PSD is filtered and the d.c. level applied to the meter circuit.

2.1 Theory

The series current through R_s and C_x is given by

$$i_o = E_o/[R_s + R_p/(1 + j\omega C_x R_p)] \quad (1)$$

where E_o is the amplitude of the applied signal and R_p the shunt or leakage resistance. If $R_s \ll R_p/(1 + j\omega C_x R_p)$ the voltage drop across R_s is

$$V_s = E_o R_s(1/R_p + j\omega C_x) \quad (2)$$

This shows that to a first approximation the quadrature or reactive component of current is independent of the loss resistance R_p. Since the pure reactive component leads by 90 degrees on the applied voltage and the loss component is in phase with the applied voltage, PSD should be a suitable technique for determining both capacitance and loss resistance.

2.2 *Phase Sensitive Detection of Reactive and Loss Components*

The basic arrangement for achieving PSD is shown in Figure 2. The output of the differential amplifier is applied to terminals AA′ and the phase detected signal obtained from terminals BB′. Switch S is arranged to close during a pre-selected period of the input signal phase. If the switch phasing lags the applied voltage E_o by 90 degrees the reactive component of the input signal will be detected. If S switches in phase with the applied voltage the loss component will be detected. In practice S is either a transistor switching circuit, a low "on" conductance F.E.T. or, for low frequency measurements (50Hz), a mercury wetted reed relay may be used to yield nearly ideal switching characteristics.

If the reactive component of current is detected the voltage appearing across the output terminals of the PSD is

$$V(I) = \omega C_x R_s E_o A \frac{\cos\theta}{\pi} \quad (3)$$

where A is the gain product of the system and θ is the phase angle of the input signal with respect to the reference signal.[1] Eq. (3) shows if ω, R_s, E_o and A remain constant then $V(I)$ is a linear function of capacitance. The loss resistance may be determined by adjusting the reference signal to be in phase with i_o. Under these conditions the detected signal is given by

$$V(R) = E_o R_s A/R_p \quad (4)$$

This result shows the loss signal to be inversely proportional to the loss resistance. By means of a suitable calibration or accurate measurements of E_o, R_s and A the loss resistance may be determined.

This brief analysis shows the PSD method to be suitable for obtaining direct measurements of capacitance and loss conductance $G_p(=1/R_p)$. The analysis also shows the reactive and loss signals to be directly proportional to the gain product of the system, the applied signal amplitude, and frequency. Hence these parameters must be well stabilised if accurate reproducible results are required.

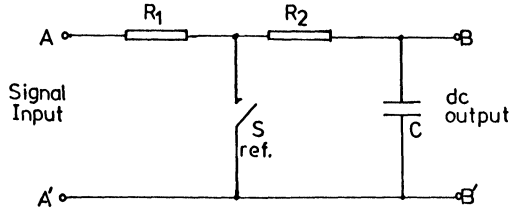

FIGURE 2 Basic circuit for phase sensitive detection. Switch S is operated by the reference phase. The signal from the main amplifier is applied to terminals AA′ and the d.c. output obtained from BB′.

3. BALLISTIC MEASURING TECHNIQUES

3.1 *Comparator Methods*

This technique relies upon the exponential rate of charge of the test specimen when driven from a step input. The time elapsed from an initial state (zero time) and a reference level is determined by means of a comparator with inputs connected between the RC_x junction and a reference voltage level, Figure 3.

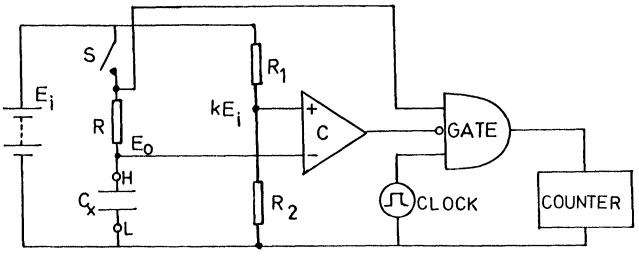

FIGURE 3 Schematic circuit diagram of a Ballistic Capacitance Meter which employs a comparator. S – specimen charging switch. C – comparator.

For a step input the voltage across C_x rises exponentially according to the relationship

$$E_o = E_i(1 - exp(-t/RC_x)) \quad (5)$$

where E_i is the input voltage step height, t the elapsed time, R the series resistance and C_x the capacitor to be tested. The time taken for the capacitor to charge

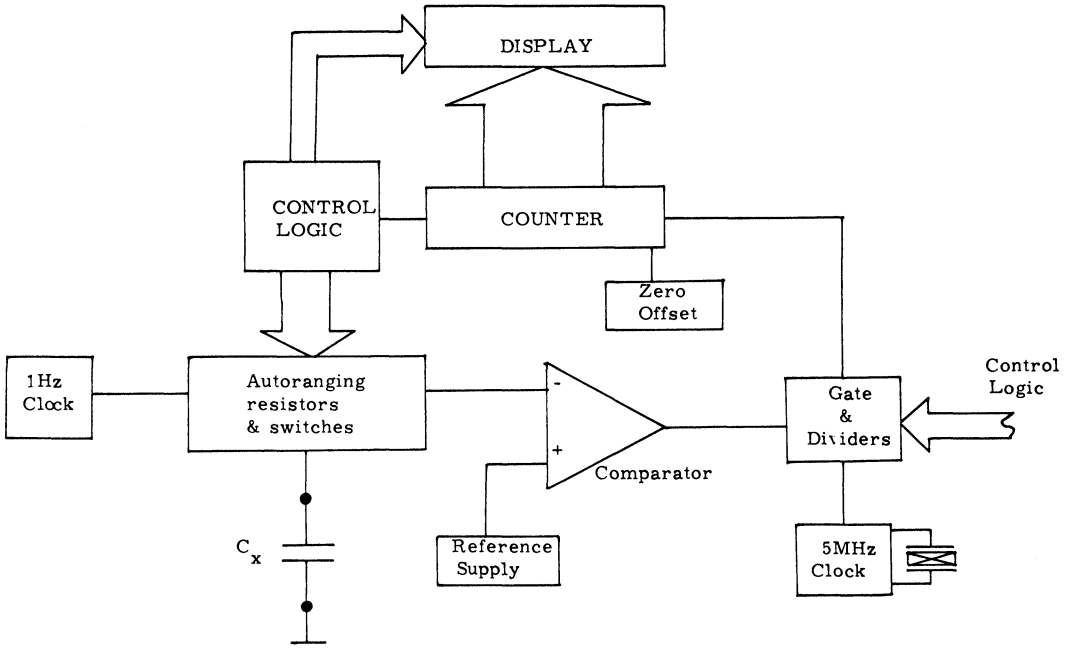

FIGURE 4(a) Schematic diagram of an autoranging ballistic capacitance meter which employs electronic switching to charge and discharge C_x.

to a reference potential kE_i is

$$T_r = -C_x R \ln(1 - E_o/E_i) \tag{6}$$

or

$$T_r = -C_x R \ln(1 - k) \tag{7}$$

where

$$k = E_o/E_i = R_2/(R_1 + R_2) \tag{8}$$

Hence the capacitor C_x may be determined in terms of T_r, R, R_1 and R_2. The period T_r may be measured by gating clock pulses into a counter, as shown in Figure 3, thus providing a digital display of capacitance. By repetitively switching S, a series of output pulses is obtained, each pulse having a period which is directly proportional to the value of C_x. The average voltage of this pulse train is also proportional to C_x thus allowing direct display of capacitance in analogue form. To obtain cyclic charge and discharge of the test specimen Warnekar and Harigovindan[2] used a mercury wetted change-over reed relay switching between E_i and earth. Although this method produces nearly ideal switching characteristics the use of the reed is limited to a frequency of about 50Hz. In addition the mercury reed is orientation sensitive. To overcome these difficulties electronic switching techniques have been developed which allow direct interfacing between the specimen to be tested and the instrument logic. Figure 4(a) shows a schematic diagram of the model 300A digital capacitance meter developed by Electronic Services and Products Limited. In this design pulses supplied from a 1Hz pulse generator provide the step function input to C_x via pre-selected auto-range resistors. The comparator

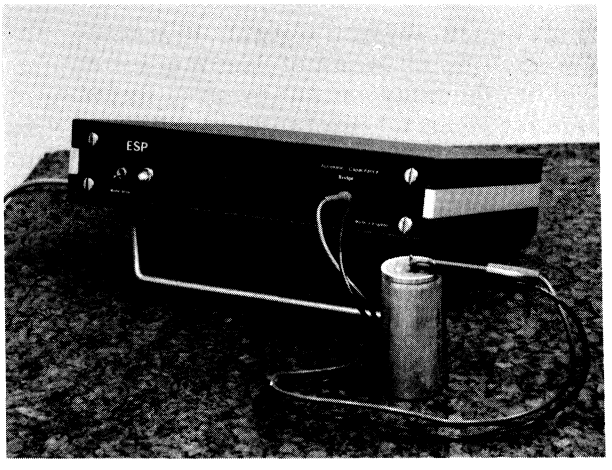

FIGURE 4(b) Direct reading ballistic capacitance meter which uses the comparator method. Autoranging 1pF to 2mF. Manufactured by Electronic Services and Products Ltd., Daventry, England. Model 300A.

senses the voltage across C_x and in conjunction with control logic signals, enables the gate. This allows clock pulses, derived from a precision 5MHz crystal oscillator, to pass into the counter. During the run-up period of E_o to the target potential, κE_i, the control logic selects appropriate range resistors and binary dividers and sets the range units to be displayed. When E_o approaches to within a few μV of κE_i the comparator changes state inhibits the gate and displays the contents of the counter. The measurement is updated during the next cycle when the positive edge of the 1 Hz clock pulse resets the counters and control logic and the negative edge provides the step drive to the test capacitor.

This approach to the measurement of capacitance produces versatile designs with potential to span the total range of practical measurements. Figure 4(b) shows such an instrument manufactured by Electronic Services and Products, model 300A, which autoranges from 1pF to 2mF. A significant advance is that measurements take place at a fixed potential of approximately 1V over the entire measuring range. This is well clear of contact potential differences thus avoiding the necessity to use 4-terminal contact jigs and clips.

3.1.1. Loss resistance measurements[2] The effect of leakage resistance R_p is to shunt the timing resistor, R. Hence, $R \rightarrow R_p/(R_p + R)$. Eq. (7) then becomes

$$T_r = -C_x R(1+a)^{-1} \ln[1 - k(1+a)] \qquad (9)$$

where

$$a = R/R_p \qquad (10)$$

If $a \ll 1$ the effect of R_p is negligible. If, however, $k(1+a) = 1$, by adjustment of either R or k, then $T_r \rightarrow \infty$ and the comparator fails to switch. By detecting this condition the factor a may be determined and a value for R_p obtained.

A particularly attractive feature of the comparator technique is that C_x is measured only in terms of time and resistance both of which may be determined to a high degree of accuracy. Since the pulse width is determined by sensing a differential input to the comparator, small changes in power supply voltage and temperature can be tolerated. Limitations of accuracy generally centre around the performance of the comparator.[2]

3.2 *Monostable Methods*

Several methods have been proposed for measuring capacitance which employ the use of monostable

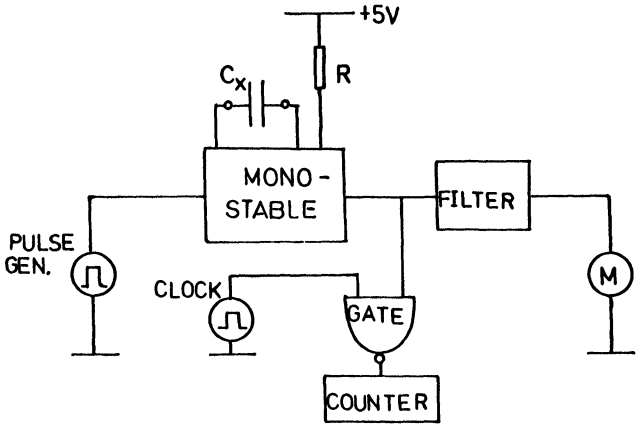

FIGURE 5 Schematic diagram of a ballistic meter which employs a monostable as the timing element.

circuits. The schematic diagram shown in Figure 5 represents a generalised version of some of these methods. In this technique a pulse generator is used to trigger the monostable which produces a train of output pulses. Each pulse has a period directly proportional to the value of the test capacitor, C_x. These pulses may be averaged to yield an analogue output voltage which is directly proportional to C_x. Alternatively, the timing pulses may be used to gate clock pulses into a counter thus providing a direct digital display of capacitance.

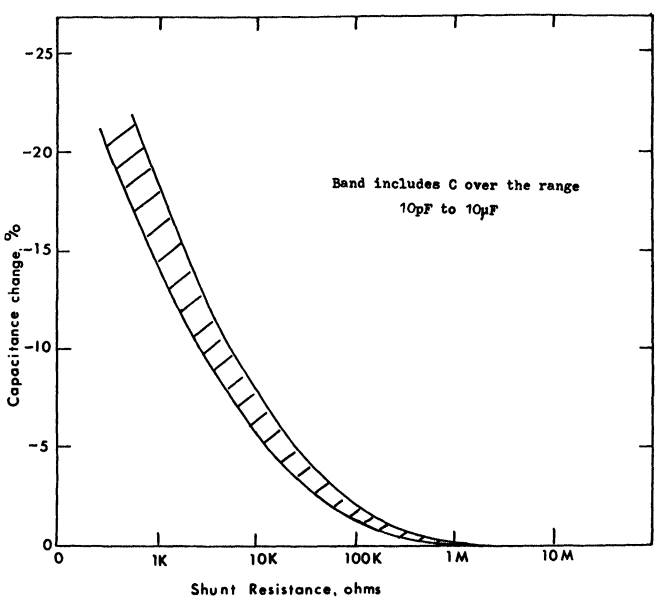

FIGURE 6 The effect of shunt (loss) resistance on capacitance reading using the monostable technique (ESP Model 100A).

The monostable used for this purpose may be designed from discrete components although integrated circuit monostables are available with excellent timing characteristics. In this case C_x is introduced into the timing circuit of the I.C. monostable. Once triggered the monostable produces a pulse of period

$$T = RC_x ln2 \qquad (11)$$

where R is the timing resistor. For I.C. monostables of type 74121, 74122 and others this linear relationship holds over at least 8 decades of capacitance change (10pF to 1mF). The effect of loss resistance in the test specimen is to shunt the timing resistor effectively reducing the output pulse width from the monostable. Since for TTL monostables the timing resistor is about 10KΩ the effect of loss resistance on accuracy only becomes significant for values of loss resistance less than 100KΩ, see Figure 6.

4. LIMITATIONS OF THE PSD AND BALLISTIC METHODS

4.1 PSD Method

Although in principle the PSD method should allow capacitance to be measured over a range 1pF>C>1F practical considerations limit the range to that shown in Figure 7. This shows a logarithmic plot of pure capacitive reactance. X_c versus capacitance. The frequencies selected correspond to those values established by BS9070 i.e. 10^6, 10^5, 10^3, 10^2 and 50Hz. The band 50Hz to 1Hz is also of interest and is discussed in the latter part of this section.

In Figure 7 two reactance limits have been drawn – one that is termed the conductance or G_p limit and the other the equivalent series resistance or ESR limit. It is possible of course to measure reactances above and below these set limits. However, for low values of reactance which approach the contact resistance of the specimen and its ESR, it is necessary to use 4-wire contacting techniques. Although these techniques may not be too troublesome when carried out in a laboratory environment the techniques are not convenient for measurements taken in the field or for high speed measurements in production.

Another, probably more important limitation, concerns the requirement to measure the capacitance of metal-insulator-semiconductor structures. In this situation it is required to measure capacitances of a few pF at frequencies as low as 5Hz. With reference to Figure 7 the reactance of such measurements is

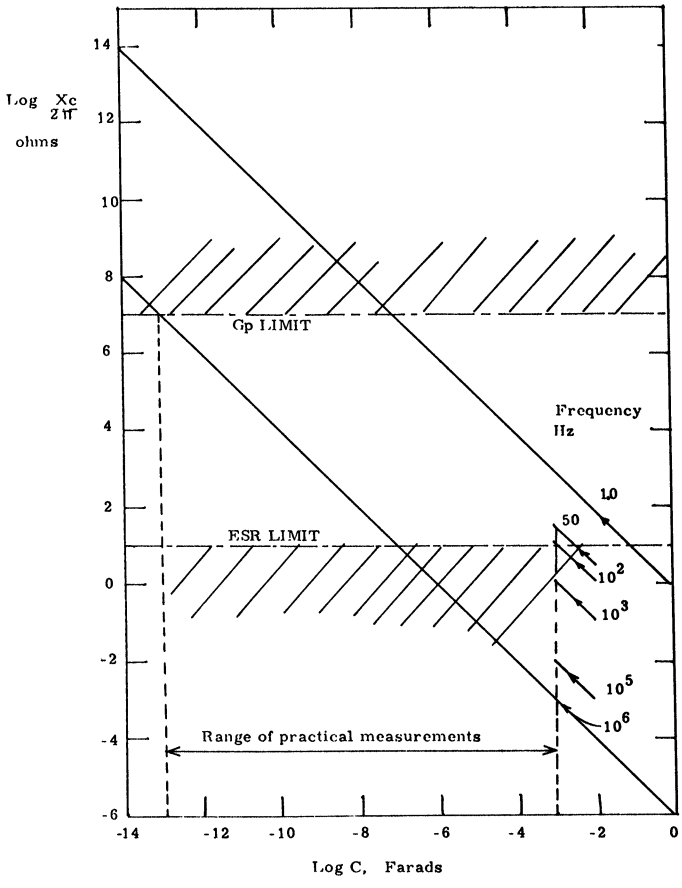

FIGURE 7 Log–Log plot of reactance vs. capacitance for a frequency band that covers BS 9070.

very high and approaches the leakage resistance of the specimens.

4.2 Ballistic Methods

In Section 3.1 Eqs. 6, 7 and 8 show that the measurement of C_x depends only upon resistance and the measurement of a time period, T_r. The latter may be determined accurately by gating clock pulses from a stable crystal oscillator into a digital counter. The value of R may be selected to correspond to the precision of measurement required. This approach has the important advantage of being directly and simply compatible with modern digital counting and display techniques. This contrasts with the PSD method which requires a further stage of analogue to digital conversion leading to further complications and loss of accuracy.

A particular limitation of the ballistic method is that measurements, as described in Section 3.1, are

nearly independant of loss resistance. However, it should be possible to obtain values of loss resistance by applying the method described in Section 3.11 and as suggested in Ref. 2. Alternatively, measurements of loss resistance may be obtained by comparing charge and discharge time constants for various values of timing resistance. A major limitation of the ballistic technique is that it is not specified as a test by BS9070. This limitation may be overcome by standardising ballistic measurements against values of capacitance determined by a.c. techniques.

The monostable method is essentially similar to the comparator method so the above considerations also apply to this method. The advantage of using a monostable is that it is a purely digital approach and as such benefits from the high reliability and low cost of TTL and CMOS logic.

5. CONCLUSIONS

An important feature, common to both ballistic measuring techniques described here, is that they are both inherently analogue to digital converters. Thus by proper choice of reference level it should be possible to measure capacitance directly with an accuracy which compares with that obtained from modern digital voltmeter techniques. This clearly contrasts with the PSD method which requires amplification and detection of analogue signals. To display such measurements in digital form requires the addition of an A/D converter with consequent loss of accuracy. In the PSD method the magnitude of the signal to be displayed depends on the total gain of the measuring system, frequency and amplitude of the driving source, and phase angle of the detected signal with respect to the reference phase. This compares with the timing period in the ballistic method which depends only on the values of fixed resistors and the switching point on the capacitor charging curve. The effect of the latter may be made negligible by choosing a high gain, fast switching comparator. However, there are two significant limitations to the ballistic method. Firstly, the design requirements to measure loss resistance are not simple, although it is considered that such design would be no more involved than that required in the PSD method. Approaches to this problem are considered in Sections 3.1.1. and 4.2. Secondly the ballistic measurement is not a test which is included in BS9070 for the testing of fixed capacitors. This applies even though the ballistic test has been used for many years for testing large value electrolytics and as a special test for capacitors used in transient switching applications. Since the use of capacitors in the latter area has now become the norm rather than the exception, the ballistic test should no longer be considered as a special test.

Significant advantages of the ballistic approach is that designs employ nearly all digital elements and the instruments benefit from high noise immunity and the elimination of 4-terminal test jigs.

6. SUMMARY

A large number of techniques for the direct measurement of capacitance has been reported in the literature.[3-7] The two essentially different approaches described here are capable of achieving most of the requirements for direct reading instruments. However, the particular method used will depend to a large extent on its application. For example the techniques which rely on a step drive to the test specimen, such as the comparator and monostable methods, do not presently provide facilities for loss factor measurements, although it is considered that these functions will shortly become available. The principal advantage of the ballistic techniques is that it is ideally suited for rapid direct measurements covering the total range of practical capacitance values.

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